## REMARKS

Reconsideration and allowance of the above-identified application, as currently amended, is respectfully requested.

By the above-made amendments, claims 3, 5, 7-8, 10 and 13 are pending, of which independent claim 3 and dependent claim 5 were amended. The revisions implemented in independent claim 3 are of a further clarifying nature including to particularly highlight the various structurally characterizing aspects of the set forth digital-control type clock data recovery circuit. In this regard, also, the set forth aspects regarding application of a plurality of results of the phase detection in terms of phase shift, such as previously contained in dependent claim 6, is now featured in independent claim 3 and as further limited with regard to dependent claim 5 thereof.

With the cancelling of claims 1-2, 4 and 12, the outstanding art rejections directed thereto have been rendered moot. It is submitted, however, agreeing to the cancelling of these claims should not be construed as acquiescence with regard to the alleged merits of those rejections. In this regard, claims 1-2, 4 and 12 were cancelled without prejudice or disclaimer of the subject matter therein.

The invention in claim 3 is a digital-control type clock data recovery circuit which comprises:

> a phase comparator comparing a phase of input data with a phase of a data recovery clock signal generated internally, outputting a DOWN signal to delay said data recovery clock signal when an edge of said input data is detected during a first term before said data recovery clock signal and outputting an UP signal to set forward the phase of

said data recovery clock signal when an edge of said input data is detected during a second term after said data recovery clock signal;

a multistage register circuit storing onset of said DOWN signal and onset of said UP signal at each of comparing opportunities during a phase detection period corresponding to a plurality of cycles of said data recovery clock signal, generating an OUT DOWN signal if at least one DOWN signal is stored at an end of the phase detection period and generating an OUT UP signal if at least one UP signal is stored at the end of the phase detection period; and

a clock-phase generation unit generating said data recovery clock signal and shifting the phase of said data recovery clock signal on the basis of the OUT UP signal and the OUT DOWN signal output from said multistage register circuit so as to separate edges of said data recovery clock signal away from edges of said input data by a predetermined time gap;

wherein said input data is taken in with a timing of said data recovery clock signal.

An illustration of this can be seen with regard to the disclosed example first embodiment described in connection with Figs. 1+ (see also Fig. 12 as combined with Fig. 1 as well as Figs. 14 and 15 relating to other disclosed example embodiments). Regarding the embodiment in Fig. 1 of the drawings, reference numerals 103, 105 and 106 are examples of the set forth phase comparator, multistage register circuit, and clock-phase generation unit, respectively. Regarding claim 5 (dependent on claim 3) and, further, regarding that set forth in claim 7, the example illustrations relating to the clock-phase generation unit 106 in Fig. 1 and that in Fig. 1 as combined with Fig. 12 (regarding the phase variable-delay circuit) are examples thereof, although not to be construed as being limited thereto.

It is submitted, the invention currently set forth in claims 3, 5, and 7-8 was neither disclosed nor suggested by Gaudet (USP 6,285,726). Supportive discussion

directed thereto follows. It can be said, arguably, that Gaudet's clock recovery architecture for recovering clock and serial data from an incoming data stream does include the comparing of the phase of input data and that of the generated clock so that the clock signal is controlled. However, the technique employed in accordance with the present invention for the recovery of the clock signal is quite different from that taught by Gaudet.

According to amended claim 3, the clock data recovery circuit controls a phase of a clock signal such that an edge of the input data is not included in the specified range from that of an edge of the clock signal, i.e., the clock data recovery circuit of the present invention effects control such that the edge of the clock is kept away from the edge of the input data. This leads to, for example, an improvement in jitter tolerance and, also, the data recovery range in the event of a wander (or phase deviation) is broadened. In order to achieve such effective control, the invention according to independent claim 3 calls for, among the set forth aspects thereof, a phase comparator that generates a DOWN signal to delay the clock when the edge of the input data appears in a first term (e.g., see term A in Fig. 4) before the data output edge of the clock signal and generates an UP signal to set forward the clock signal when the edge of the input data appears in the second term (e.g., term B in Fig. 4) after the data output edge of the clock. This is now set forth in claim 3 as follows:

> a phase comparator comparing a phase of input data with a phase of a data recovery clock signal generated internally, outputting a DOWN signal to delay said data recovery clock signal when an edge of said input data is detected during a first term before said data recovery

clock signal and outputting an UP signal to set forward the phase of said data recovery clock signal when an edge of said input data is detected during a second term after said data recovery clock signal.

Also, according to claim 3, the clock data recovery circuit of the invention calls for a multistage register circuit, an example of which is shown by reference numeral 105 in Fig. 1 of the drawings and also, more specifically, in Fig. 10 of the drawings, although not to be construed as being limited thereto. In accordance with claim 3, the multistage register circuit is such that it *stor[es] onset of said DOWN signal and onset of said UP signal at each of comparing opportunities during a phase detecting period (e.g., Tp in Fig. 2) corresponding to a plurality of cycles of said data recovery clock signal, generating an OUT DOWN signal if at least one DOWN signal is stored at an end of the phase detection period and generating an OUT UP signal if at least one UP signal is stored at the end of the phase detection period, in order to apply to the clock phase.*

It is submitted a schemed clock data recovery circuit as that set forth in claim 3 and, correspondingly, also in the dependent claims thereof, was neither disclosed nor suggested in view of Gaudet.

The clock data recovery circuit, such as shown in Fig. 5 of Gaudet features phase comparators, including a rising edge phase comparator (e.g., 114) and a falling edge phase comparator (e.g., 115). It is submitted, however, that Gaudet does not employ a phase comparison in the manner as that presently set forth in independent claim 3 and as more particularly defined in the corresponding dependent claims. In this regard, it is noted that Gaudet does not describe nor

suggest operating a phase comparator to control the delay of or set forward the clock signal on the basis of whether *an edge of the input data is detected during the first term before the data recovery clock signal or when an edge of the input data is detected during the second term after the data recovery clock signal*. Judging from the description "[t]his acts to bring the clock signal into phase with the data" (see column 6, lines 58-59, in Gaudet), it seems that Gaudet's architecture calls for effecting control so as to match the edge of the clock to the edge of the data, in clear contradistinction with that according to claims 3+.

It is submitted, also, that Gaudet neither disclose nor suggested a schemed construction in which detected signals at each of the comparing opportunities during the phase detection period, corresponding to a plurality of cycles of a data recovery clock ,are stored and that they are applied towards phase control, consistent with that presently set forth.

For at least the above reasons, the invention according to independent claim 3 and, likewise, according to dependent claims 5, 7 and 8, could not have been anticipated from Gaudet nor, for that matter, achievable in view of Gaudet's teachings. Applicants also consider the invention as defining over the other art documents of record.

Therefore, in view of the above-made amendments, together with the accompanying Remarks, withdrawal of the outstanding rejections, as well as favorable action on the currently pending claims together with an early formal notification of allowance of the above-identified application is respectfully requested.

**STATEMENT OF SUBSTANCE OF INTERVIEW**

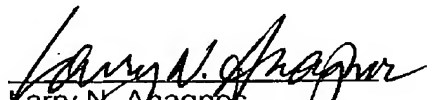
This statement is to report the telephone discussion held with the Examiner on December 11, 2007, subsequent to receiving the outstanding Office Action, which is dated November 14, 2007. In reviewing the Examiner's Detailed Action therein, a discrepancy was observed regarding the status of the Official Action, namely, according to the Office Action Summary Sheet (Form PTOL-326), the outstanding Office Action is a non-final Office Action on the merits (see Item 2b). However, on page 9 of the Official Action, the Examiner indicated that this action is a Final Office Action on the merits (see Item 13 of the Detailed Action). Accordingly, Applicant's undersigned representative telephoned the Examiner for purposes of receiving clarification from him as to the status of this Official Action. The Examiner reviewed the Official Action on the PTO website and indicated that an inadvertent error was made in the Office Action. According to the Examiner, the present action is correctly indicated in Form PTOL-326 as being a non-final Office Action and that Item 13 on page 9 of the Official Action was entered in error. In this regard, the Examiner also noted that the official PTO website shows that the present Office Action was in fact docketed as a non-final Office Action and, according to the Examiner, should be considered by Applicants as such. This ended the discussion at that time. The Examiner is thanked for this clarification.

To the extent necessary, Applicants petition for an extension of time under 37 C.F.R. §1.136. Please charge any shortage in fees due in connection with the

filing of this paper, including extension of time fees, to the Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (Docket No. 520.43305X00), and please credit any excess fees to such deposit account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

By 
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